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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,244	08/24/2001	Michael Dibrino	SC11317TH	2202

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/939,244	Applicant(s) DIBRINO, MICHAEL
	Examiner Chat C. Do	Art Unit 2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 24 August 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/24/04.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the applicant is advised to update information in related application section page 1 wherein the U.S. Serial No. 09/542,016 is abandoned.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-7, 9-11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al. (U.S. 6,275,838) in view of Zou et al. (U.S. 6,425,070).

Re claim 1, Blomgren et al. disclose in Figure 8B a floating point multiplier and accumulator for repetitively performing multiplication and addition operations to create a product of a first operand (800c) and a second operand (800b) and adding a third operand (800a) to the product, comprising: a multiplier array (832) having a first input and a second input for respectively receiving the first operand and the second operand, and providing a sum and a carry (outputs of 832); shifting circuitry (830) for receiving the third operand and selectively bit shifting the third operand; adder circuitry (834) coupled

to the shifting circuitry (830), the adder circuitry adding the sum, the carry (outputs of 832) and the third operand (output 830) to provide at an output thereof a mantissa portion of a resultant operand that has not been normalized or rounded (output of 834); and feedback circuitry (812) coupled to the adder circuitry and the multiplier array, the feedback circuitry coupling the mantissa portion of the resultant operand to either the multiplier array or the shifting circuitry to be subsequently used as one of the first operand, the second operand or the third operand, such feedback being done without first performing normalization or rounding (before entering 803), thereby reducing latency associated with creating the product when one of the first operand, the second operand or the third operand has a value that is dependent upon a previous resultant operand calculated by the floating point multiplier (832) and accumulator (834). Blomgren et al. do not disclose a multiplexor circuitry coupled to the multiplier array for selectively bit shifting each of the sum and the carry. However, Zou et al. disclose in Figure 8 a multiplexor circuitry coupled to the multiplier array for selectively bit shifting each of the sum and the carry (904 wherein the instruction decode is used to make a decision of shifting and select the output of the shifter). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a multiplexor circuitry coupled to the multiplier array for selectively bit shifting each of the sum and the carry as seen in Zou et al.'s Figure 8 into Blomgren et al.'s Figure 8B because it would enable to a faster correct result of multiply and accumulate by aligning the operands into proper position for addition/subtraction.

Re claim 2, Blomgren et al. further disclose in Figure 8B the adder circuitry further comprises a carry save adder (first adder in 834) having a first input for receiving the sum, a second input for receiving the carry (output of 832), and a third input for receiving the third operand (output of 830), a first output for providing a sum output, and a second output for providing a carry output (output of the first adder in 834), and a carry propagate adder (second adder in 834) having a first input coupled to the sum output of the carry save adder, a second input coupled to the carry output of the carry save adder (outputs of the first adder in 834), and an output for providing the resultant operand (output of second adder in 834).

Re claim 3, Blomgren et al. further disclose in Figure 8B a normalizer (803) coupled to the output of the adder circuitry, the normalizer removing leading edge zeroes from the resultant operand after the resultant operand has been fed back to be used as one of the first operand, the second operand or the third operand in a subsequent calculation of the floating point multiplier and accumulator.

Re claim 5, Blomgren et al. further disclose in Figure 8B a first register (800b) for receiving and selectively storing either the first operand or the resultant operand, the first register being coupled to the first input of the multiplier array, the first register selecting either the first operand or the resultant operand in response to execution of an operational code; and a second register for receiving and selectively storing either the second operand or the resultant operand, the second register (800c) being coupled to the second input of the multiplier array, the second register selecting either the second operand or the resultant operand in response to execution of the operational code.

Re claim 6, Blomgren et al. do not disclose in Figure 8B first control circuitry coupled to the multiplexor circuitry for controlling bit shifting of the sum and carry generated by the multiplier array, the first control circuitry performing predetermined calculations to determine a bit shift amount to shift the sum and carry; and second control circuit coupled to the shifting circuitry for controlling an amount of shifting performed by the shifting circuitry. However, Zou et al. disclose in Figure 8 first control circuitry coupled to the multiplexor circuitry for controlling bit shifting of the sum and carry generated by the multiplier array, the first control circuitry performing predetermined calculations to determine a bit shift amount to shift the sum and carry; and second control circuit coupled to the shifting circuitry for controlling an amount of shifting performed by the shifting circuitry (col. 16 lines 10-17 from instruction decode 158). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to first control circuitry coupled to the multiplexor circuitry for controlling bit shifting of the sum and carry generated by the multiplier array, the first control circuitry performing predetermined calculations to determine a bit shift amount to shift the sum and carry; and second control circuit coupled to the shifting circuitry for controlling an amount of shifting performed by the shifting circuitry as seen in Zou et al.'s Figure 8 into Blomgren et al.'s Figure 8B because it would enable to improve the system performance (col. 16 lines 52-54).

Re claim 7, Blomgren et al. further disclose in Figure 8B exponent generation circuitry (870) for generating an exponent value of the resultant operand based upon an

internal exponent value and a number of leading zeroes contained in the resultant operand.

Re claims 9-10, Blomgren et al. do not disclose in Figure 8B the shifting circuitry further comprises a right shifter that selectively bit shifts the third operand or the resultant operand in response to predetermined calculations that determine a bit shift amount, if any, to implement and the multiplexor circuitry bit shifts each of the sum and carry by a number of bits that is determined, in part, by a number of leading zero bits of the resultant operand from a previous calculation performed by the multiplier array. However, Zou et al. disclose the shifting circuitry further comprises a right shifter that selectively bit shifts the third operand or the resultant operand in response to predetermined calculations that determine a bit shift amount, if any, to implement (900) and the multiplexor circuitry bit shifts each of the sum and carry by a number of bits that is determined, in part, by a number of leading zero bits of the resultant operand from a previous calculation performed by the multiplier array (904). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the shifting circuitry further comprises a right shifter that selectively bit shifts the third operand or the resultant operand in response to predetermined calculations that determine a bit shift amount, if any, to implement and the multiplexor circuitry bit shifts each of the sum and carry by a number of bits that is determined, in part, by a number of leading zero bits of the resultant operand from a previous calculation performed by the multiplier array as seen in Zou et al.'s Figure 8 into Blomgren et al.'s Figure 8B because

it would enable to improve the system performance (col. 16 lines 52-54) by properly aligned the operand with the output of multiplication.

Re claim 11, it is an integrated circuit claim of claim 1. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of claim 1.

Re claim 13, it is an integrated circuit claim of claim 7. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of claim 7.

Re claim 14, it is a method claim of claim 1. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of claim 1.

4. Claims 4, 8, 12, and 15 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al. (U.S. 6,275,838) in view of Zou et al. (U.S. 6,425,070) as applied to claim 1 above, and further in view of Montoye et al. (U.S. 4,969,118).

Re claim 4, Blomgren et al. in view of Zou et al. do not disclose in Figures 8 and 8B a selective inverter coupled to the output of the adder circuitry, the selective inverter changing a logic value of each bit of the resultant operand in response to determining that the resultant operand has a negative sign, selective inversion occurring prior to feeding the mantissa portion of the resultant operand back to the multiplier array but without normalization or rounding of the resultant operand. However, Montoye et al. disclose in Figure 1 a selective inverter (22) coupled to the output of the adder circuitry (18), the selective inverter changing a logic value of each bit of the resultant operand in response to determining that the resultant operand has a negative sign (col. 5 lines 6-12), selective inversion occurring prior to feeding the mantissa portion of the resultant operand back to

the multiplier array but without normalization or rounding of the resultant operand. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a selective inverter coupled to the output of the adder circuitry, the selective inverter changing a logic value of each bit of the resultant operand in response to determining that the resultant operand has a negative sign, selective inversion occurring prior to feeding the mantissa portion of the resultant operand back to the multiplier array but without normalization or rounding of the resultant operand as seen in Montoye et al.'s Figure 1 into Blomgren et al. in view of Zou et al.'s Figures 8 and 8B because it would enable to handle signed numbers (col. 5 lines 21-23).

Re claim 8, Blomgren et al. disclose in Figure 8B a register (800a) for receiving and selectively storing the third operand or the resultant operand. Blomgren et al. in view of Montoye et al. do not disclose in Figure 8 nor 8B a selective inverter coupled to the register for selectively inverting a logic state of each bit position of each value stored in the register based upon a sign of each value, the selective inverter having an output coupled to the shifting circuitry. However, Montoye et al. disclose in Figure 1 a selective inverter (20) coupled to the register for selectively inverting a logic state of each bit position of each value stored in the register based upon a sign of each value, the selective inverter having an output coupled to the shifting circuitry. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a selective inverter (20) coupled to the register for selectively inverting a logic state of each bit position of each value stored in the register based upon a sign of each value, the selective inverter having an output coupled to the shifting circuitry as seen in

Montoye et al.'s Figure 1 into Blomgren et al. in view of Zou et al.'s Figures 8 and 8B because it would enable to improve the system performance of adding a negative operand in one complement by complementing the negative operand.

Re claim 12, it is an integrated circuit claim of claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of claim 4.

Re claim 15, it is a method claim of claim 4. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of claim 4.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,185,713 to Kobunaya discloses a product adder for performing multiplication of floating point data and addition of fixed point data.

b. U.S. Patent No. 5,517,436 to Andreas et al. disclose a digital signal processor for audio applications.

c. U.S. Patent No. 5,450,607 to Kowalczyk et al. disclose an unified floating point and integer datapath for a RISC processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

July 9, 2004

Kakali Chaki

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